REMARKS

Claims 1-5 and 10-14 are rejected, as set forth below. Claims 6-9 are cancelled, without prejudice or disclaimer, and claim 5 has been amended in response to Examiner request in the Office action. Applicants respectfully submit that the claims, as previously filed and currently amended in claim 5, are in condition for allowance and respectfully request reconsideration in view of the following.

Rejections under 35 U.S.C. §102(e)

Claims 1-13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent 6,983,398 (*Prabhu*). At least for the reasons discussed below, applicants respectfully submit that the claims, as originally filed, patentably distinguish over *Prabhu*.

In the Office action, the Examiner cites to column 3, lines 22-27 and column 5, line 64 to column 6, line 32 for the proposition that *Prabhu* anticipates claims 1-13. Provided below for the Examiner's convenience are the cited portions of *Prabhu*. Specifically, column 3, lines 22-27 of *Prabhu* states:

> One or a set of various processors 110 tests one or a set of processors 110. One processor 110 may perform some tests while a processor 110 compares and analyzes the test results. Consequently, testing chip 100 may be referred to as "self-test" because chip 100 conducts tests using its own elements.

And, column 5, line 64 to column 6, line 32 of *Prabhu* states:

> In one embodiment, a processor 110 executes its corresponding test program independent of other processors. Each processor 110 starts and/or stops its program any time, at irregular intervals, and/or without other processors knowing about it, as long as the test results are available to be analyzed when analyzing the test results starts. The processors' system clocks do not have to be cycle locked, e.g., one clock does not depend on another clock, etc. For example, a processor 110-1 may run its program in series or in parallel with a processor 110-2; processor 110-1 may stat at time t1 and stop at time t2 while processor 110-2 starts at time t3 and stops at time t4 wherein times t1, t2, t3, and t4 are different and independent of one another, etc. However, t1 is less than or equal to t2. Similarly, t3 is less than or equal to t4. Since, in one embodiment, each processor 110 corresponds to a test program and each test program can provide different tests, one processor 110 can run different tests from another processor 110 or analyze test results provided by other processors 110. For example, a processor 110-1 is testing a floating-point unit for a processor 110-2, while a processor 110-3 is testing an integer unit for a processor 110-4, and processor 110-5 compares the test results provided by processors 110-2 and 110-3, etc. In one embodiment, once a processor 110 finishes its test program, that processor sets a flag at a corresponding memory location so that other processors can take appropriate actions. For example, once each processor 110-1 and 110-2 finishes

testing processor 110-3, each processor 110-1 and 110-2 sets a flag corresponding to the programs that each has executed. Processor 110-4, recognizing the flags of processors 110-1 and 110-2 have been set, starts running its program to analyze the test results provided by these processors 110-1 and 110-2. In an alternative embodiment, a processor 110 sets a flag when some portions of the test programs were executed so that the completed test results may be analyzed while additional tests are being executed.

After reviewing carefully the above-cited passages, applicants respectfully submit that they do not disclose each and every claim limitation found in applicants' independent claims 1 and 10. For example, independent claim 1 recites:

> performing the first self test process in response to a first actuation of a test control by a user of the system.

Thus, independent claim 1 requires the performance of the first test process "in response to a first actuation of a test control by a user of the system." The cited passages from *Prabhu* nowhere disclose or in any way suggest "actuation of a test control by a user," thereby failing to anticipate claim 1.

Additionally, independent claim 1 recites:

> performing the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time.

Independent claim 1 therefore requires the performance of the second test process "in response to a second actuation of the test control prior to lapse of a first predefined period of time." The cited passages from *Prabhu* nowhere disclose or in any way suggest performance of the second test process "in response to a second actuation of the test control prior to lapse of a first predefined period of time," again failing to anticipate claim 1.

Moreover, independent claim 1 recites:

> terminating the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time.

Accordingly, independent claim 1 requires the termination of the second self test process "in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time." The cited passages from *Prabhu* nowhere disclose or in any way suggest termination of the second self test process "in response to a third actuation of the test control by the user of the system, wherein the

third actuation is maintained for more than a second predetermined period of time," yet again failing to anticipate claim 1.

Regarding independent claim 10, applicants respectfully submit that arguments similar to those described above can be made, and for that reason, the rejection of claim 10 is improper.

For at least the above-stated reasons, applicants respectfully submit that *Prabhu* fails to anticipate claims 1-13 and therefore request the allowance of the remaining pending claims thereof.

Rejections under 35 U.S.C. §103(a)

Claim 14 is rejected under 35 U.S.C. 103(a) as being obvious over *Prabhu* in view of U.S. patent publication 2006/0273929 (*Tran*). Applicants respectfully submit that *Tran* fails to rectify the above-stated shortcomings of *Prabhu*, and therefore, the cited combination fails to render obvious claim 14. Applicants therefore respectfully request the allowance of claim 14.

Rejection under 35 U.S.C. § 101

Claims 5 and 6-9 are rejected under 35 § 101 as allegedly being directed to non-statutory subject matter. Claim 5 has been amended, as suggested by the Examiner, thereby traversing this rejection, while claims 6-9 have been cancelled, without prejudice or disclaimer, thereby rendering this rejection moot.

Rejection Under 35 U.S.C. §112, Second Paragraph

Claim 6 is rejected under 35 U.S.C. §112 as having insufficient antecedent basis for the limitations "the first self test" and "the second self test." Claims 6-9 have been cancelled, without prejudice or disclaimer, thereby rendering this rejection moot.

CONCLUSION

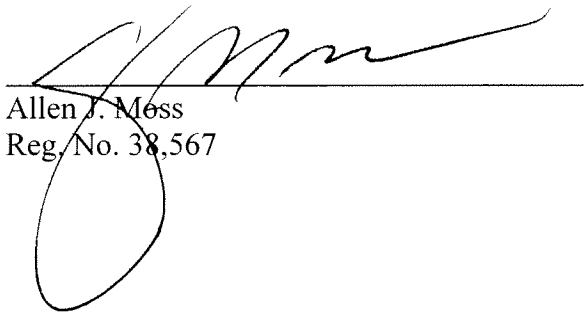
Reconsideration is respectfully requested. Applicants believe the case is in condition for allowance and respectfully request withdrawal of the rejections and allowance of the pending claims.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to **Deposit Account No. 19-3878**.

The Examiner is invited to telephone the undersigned at the telephone number listed below if it would in any way advance prosecution of this case.

Respectfully submitted,

Date: July 12, 2007



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